

WHAT IS CLAIMED IS:

- 1 1. A peer-vector machine, comprising:
2 a host processor operable to execute a program, and, in response to the
3 program, operable to generate first host data; and
4 a pipeline accelerator coupled to the host processor and operable to receive the
5 first host data and to generate first pipeline data from the first host data.
- 1 2. The peer-vector machine of claim 1 wherein the host processor is further
2 operable to:
3 receive second data; and
4 generate the first host data from the second data.
- 1 3. The peer-vector machine of claim 1 wherein the host processor is further
2 operable to:
3 receive the first pipeline data from the pipeline accelerator; and
4 process the first pipeline data.
- 1 4. The peer-vector machine of claim 1 wherein the host processor is further
2 operable to:
3 receive the first pipeline data from the pipeline accelerator; and
4 generate the first host data from the first pipeline data.
- 1 5. The peer-vector machine of claim 1, further comprising:
2 an interface memory coupled to the host processor and to the pipeline
3 accelerator and having a first memory section;
4 wherein the host processor is operable to,
5 store the first host data in the first memory section, and
6 provide the first host data from the first memory section to the pipeline
7 accelerator.
- 1 6. The peer-vector machine of claim 1, further comprising:
2 an interface memory coupled to the host processor and to the pipeline
3 accelerator and having first and second memory sections;
4 wherein the host processor is operable to,

5 store the first host data in the first memory section,
6 provide the first host data from the first memory section to the pipeline
7 accelerator,
8 receive the first pipeline data from the pipeline accelerator,
9 store the first pipeline data in the second memory section,
10 retrieve the first pipeline data from the second memory section to the host
11 processor, and
12 process the first pipeline data.

1 7. The peer-vector machine of claim 1 wherein the host processor is
2 operable to configure the pipeline accelerator.

3 8. The peer-vector machine of claim 1 wherein the pipeline accelerator
4 comprises a programmable-logic integrated circuit.

1 9. A peer-vector machine, comprising:
2 a pipeline accelerator operable to generate first pipeline data; and
3 a host processor coupled to the pipeline accelerator and operable to execute a
4 program and, in response to the program, operable to receive the first pipeline data and
5 to generate first host data from the first pipeline data.

1 10. The peer-vector machine of claim 9 wherein the pipeline accelerator is
2 further operable to:
3 receive second data; and
4 generate the first pipeline data from the second data.

1 11. The peer-vector machine of claim 9 wherein the pipeline accelerator is
2 further operable to:
3 receive the first host data from the host processor; and
4 process the first host data.

1 12. The peer-vector machine of claim 9 wherein the pipeline accelerator is
2 further operable to:
3 receive the first host data from the host processor; and
4 generate the first pipeline data from the first host data.

1 13. The peer-vector machine of claim 9, further comprising:
2 an interface memory coupled to the pipeline accelerator and to the host
3 processor and having a first memory section; and
4 wherein the host processor is operable to,
5 store the first pipeline data from the pipeline accelerator in the first
6 memory section, and
7 retrieve the first pipeline data from the first memory section.

1 14. The peer-vector machine of claim 9, further comprising:
2 an interface memory coupled to the pipeline accelerator and to the host
3 processor and having first and second memory sections;
4 wherein the host processor is operable to,
5 store the first pipeline data from the pipeline accelerator in the first
6 memory section,
7 retrieve the first pipeline data from the first section,
8 store the first host data in the second memory section, and
9 provide the first host data from the second memory section to the pipeline
10 accelerator; and
11 wherein the pipeline accelerator is operable to process the first host data
12 received from the second memory section.

1 15. The peer-vector machine of claim 9 wherein the host processor is
2 operable to configure the pipeline accelerator.

1 16. A system, comprising:
2 a device operable to generate raw data;
3 a host processor coupled to the device and operable to execute a program, and,
4 in response to the program, operable to generate host data from the raw data; and
5 a pipeline accelerator coupled to the host processor and operable to receive the
6 host data and to generate pipeline data from the host data.

1 17. A system, comprising:
2 a device operable to generate raw data;

3 a pipeline accelerator coupled to the device and operable to generate pipeline
4 data from the raw data; and

5 a host processor coupled to the pipeline accelerator and operable to execute a
6 program and, in response to the program, operable to receive the pipeline data and to
7 generate host data from the pipeline data.

1 18. A method, comprising:

2 generating first host data by executing a program with a host processor; and
3 generating first pipeline data from the first host data with a pipeline accelerator.

1 19. The method of claim 18, further comprising:

2 receiving raw data;

3 wherein generating the first host data comprises generating the first host data
4 from the raw data.

1 20. The method of claim 18 wherein generating the first host data comprises
2 generating the first host data from the first pipeline data.

1 21. The method of claim 18, further comprising generating second host data
2 from the first pipeline data by executing the program with the host processor.

1 22. The method of claim 18, further comprising configuring the pipeline
2 accelerator by executing the program with the host processor.

1 23. A method, comprising:

2 generating first pipeline data with a pipeline accelerator; and

3 generating first host data from the first pipeline data by executing a program with
4 a host processor.

1 24. The method of claim 23, further comprising:

2 receiving raw data;

3 wherein generating the first pipeline data comprises generating the first pipeline
4 data from the raw data.

1 25. The method of claim 23 wherein generating the first pipeline data
2 comprises generating the first pipeline data from the first host data.

1 26. The method of claim 23, further comprising generating second pipeline
2 data from the first host data with the pipeline accelerator.

1 27. The method of claim 23, further comprising configuring the pipeline
2 accelerator by executing the program with the host processor.